UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/523,666	02/04/2005	Jose De Jesus Pineda De Gyvez	NL 020835	8446

24737 7590 06/16/2006

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/523,666	PINEDA DE GYVEZ ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-11,13-15 and 17* is/are rejected.

7)☒ Claim(s) *2,3,12 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4-11, 13-15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marr et al. (USP 6529421) in view of Lee et al. (USP 5223753) and Cave et al. (USP 5087830).

Marr et al.'s figure 20A shows a threshold control circuit, but does not show the detail of the bandgap voltage generator 2018 and the detail of comparator 2010. However, Lee et al.'s figure 2 shows a comparator circuit and Cave et al.'s figure 1 shows a bandgap voltage generator both having low power consumption. Therefore, it would have been obvious to one having ordinary skill in the art to use Lee et al.'s comparator and Cave et al.'s bandgap circuit for Marr et al.'s comparator and bandgap circuit for the purpose of saving power consumption. Thus the modified Marr et al.'s figure 20A shows: a control unit controlling a threshold voltage of a circuit unit (2002) having a plurality of transistor devices, comprising a reference circuit (Cave et al. figure 1 in the modified 2018); a measuring unit (Lee et al.'s 1-3, 5 and 6 in the modified 2010) measuring a threshold voltage of at least one sensing transistor of the circuit unit and measuring a reference threshold voltage of at least one reference transistor of the reference circuit; a differential voltage generator (Lee et al.'s 4 and 7-13 in the modified 2010) generating

a differential voltage from outputs of the measuring unit and a bulk connection of the transistor devices in the circuit unit to which the differential voltage is fed as a biasing voltage.

As to claim 4, the modified Marr et al. shows the reference circuit comprises at least one reference transistor (Cave's 46) in at least one comparator amplifier (Cave's 16).

As to claim 5, it would have been obvious to one having ordinary skill in the art to the reference transistor to be provided in a separate well of the chip comprising the circuit unit in order to separate temperature characteristic between two circuits.

As to claim 6, the modified Marr et al.'s figure 20A shows that the reference transistor is controlled separately from the transistor devices of the circuit unit by a reference voltage.

As to claim 7, the modified Marr et al. shows that the measuring unit comprises at least one sensing transistor (Lee et al.'s 1) sensing the threshold voltage.

As to claim 8, the modified Marr et al.'s figure 20A shows that the sensing transistor is controlled separately from the reference transistor by a sensing voltage.

As to claim 9, the modified Marr et al.'s figure 20A shows the circuit unit comprises a plurality of transistor devices (transistors in 2002 and transistors in Cave's figure 1, and a first sub-plurality of the transistor devices is employed as reference transistors and a second sub-plurality of the transistor devices is employed as sensing transistors, and wherein the differential output of the differential voltage generator is fed as a biasing voltage to the bulk of the plurality of transistor devices.

As to claim 10, the modified Marr et al. is integrated circuit (IC) device.

As to claim 11, the modified Marr et al.'s figure 20A shows a method for controlling of at least one threshold voltage of transistors (2002) in a circuit unit comprising: measuring (by

Lee et al.'s 1, -3, 5, 6) at least one transistor threshold voltage of the circuit unit; providing at least one reference transistor (Cave et al.'s 46) and measuring a threshold voltage of the at least one reference transistor; generating a differential voltage (Lee et al.'s Vout) from outputs (gates of 4, 9) of the measuring unit and feeding the differential voltage as a biasing voltage to a bulk connection of the transistor devices in the circuit unit.

As to claim 13, the modified Marr et al.'s figure 20A shows a plurality of transistor devices is divided up into a first sub-plurality of reference transistors and a second sub-plurality of sensing transistors and wherein the transistor threshold voltage of the first sub-plurality is measured as reference voltage; the threshold voltage of the second sub-plurality is measured as sensing voltage; a differential voltage is generated from the reference voltage and the sensing voltage and wherein the differential voltage is input to the bulk of the plurality of transistor devices (see the rejection of claim 9).

As to claim 14, the modified Marr et al.'s figure 20A shows step of the controlling of at least one threshold voltage of transistors in a circuit unit is done in a closed loop.

As to claim 15, the modified Marr et al.'s figure 20A shows the step of the controlling in the closed loop includes a controlling of a power supply (Vbb).

As to claim 17, the modified Marr et al.'s figure 20A shows that the threshold voltage is directly measured.

Allowable Subject Matter

3. Claims 2, 3, 12 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2, 3, 12 and 16 would be allowable because the prior art fails to teach or suggest that the differential voltage generator comprises: an averaging unit forming at least one average threshold voltage value of at least one measured transistor threshold voltage of the circuit unit; a comparing unit comparing at least one average threshold voltage value of the circuit unit with at least one measured transistor threshold voltage of the reference circuit and creating at least one difference voltage value indicating the difference between at least one average threshold voltage value of the circuit unit and at least one transistor threshold voltage of the reference circuit; an amplifier unit amplifying at least one difference voltage value of the comparing unit and creating at least one amplified difference voltage value.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

June 13, 2006